Novel Universal Current-mode Biquad Filter with Three Iputs and One Output Employing Minimum Active and Passive Components

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Abstract

A new universal current-mode biquad with three inputs and one output using only one fully differential second-generation current conveyor (FDCCII), two grounded capacitors and two resistors is proposed. The proposed circuit offers the following advantageous features: realization of five generic current-mode filter signals from the same configuration, no requirements of component matching conditions, employment of minimum active and passive components, employment of two grounded capacitors ideal for integrated circuit implementation, high output impedance good for cascadability, and low passive sensitivity performance. Moreover, HSPICE simulation results confirm the theoretical analysis.

Keywords: Active filters, Current conveyors, Analogue electronics

使用最少的主動與被動元件來設計電流式三輸入單輸出萬用二階濾波電路

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中文摘要

本論文提出只使用單一第二代完全差動電流傳輸器，二個接地電容及二個電阻來設計電流式三輸入單輸出萬用二階濾波電路。所提出的電路具有以下之優點：在同一個電路結構下可實現五種濾波信號，不需要任何的匹配條件及使用最少的主動與被動元件，且使用兩個接地電容有利於電路的積體化，並具有高輸出阻抗端有利於輸出電流之串接及具有非常低的被動靈敏度。最後，使用 HSPICE 來驗證電路之結果與理論可行性。

Ⅰ. Introduction

In recent two decades, there are much more attention about both employing minimum current conveyor and passive components in analog circuit design. It is well known that current conveyors can provide some advantages as follows [1]:

1. higher bandwidth capability;
   Bipolar junction transistors and FET transistors are both current output devices. A key performance feature of current mode processing is inherent wide bandwidth, and in a current conveyor of transistors is useful almost up to its unity-gain bandwidth. It can use the stray capacitances as a gain element at high frequency.
2. less complexity for analog Arithmetic;
   In the current domain, computation like addition and subtraction can be easily realized directly by joining the terminals at a single point employing current-mirror techniques.
   In contrast to the voltage-mode counterpart that needs an operational amplifier for realizing the same function.
3. wider dynamic range;
   The supply voltage has to be reduced in order to ensure device reliability as soon as the shrinking device size of integrated technology. The reduced voltage supply levels result in reduced dynamic range. Therefore, the signal range is no longer directly restricted by the supply voltage but dependent on the impedance level through the current signal representation.
4. higher operating speed;
   The shrinking dimensions of integrated circuit techniques yield to the parasitic effect of the circuit is capacitive action. Current-mode circuit can achieve high speed signaling at low impedance internal nodes and low voltage swing due to minimal capacitive charging and discharging.

In addition, it is well known that the circuits with the minimum components have much more attractive attention as follows:

1. less circuit complexity,
2. possibility less power consumption ,
3. low cost,
4. low space,
5. reduced noise,
6. less parasitic effects,
7. minimal fault chances.

Recently, the applications and advantages in the realization of various active filter transfer functions using current conveyors have received considerable attention [2]. Some universal current-mode biquads with three inputs and one output were proposed [3-7]. In 1997, C. M. Chang [3] proposed a universal active current filter with three inputs and one output employing five plus-type current conveyors (CCIIs). In 1999, Günes et al. [4] proposed a good insensitive universal current-mode filter with four inputs and one output employing three dual–output CCIIs. In the same year, Toker et al. [5] proposed a current-mode KHN-equivalent biquad employing three current differencing buffered amplifiers. In 2001, Chang et al. [6] proposed a universal current-mode filter with four inputs and one output employing three unity-gain cells. In the same year, Wang and Lee [7] proposed a good versatile insensitive current-mode universal biquad with three inputs and one output employing two dual–output CCIIs and one dual–output CCIII. However, none of the above proposed filters used minimum active and passive components. In 2004, Sharma and Senani proposed a universal current mode biquad with three inputs and one output employing a single current feedback op-amp (CFOA), two capacitors and three resistors [8]. But, the proposed configuration could not be employing grounded capacitors, and needed some match conditionals to realize high-pass, notch and all-pass filters. In this paper, the authors proposed a novel advanced universal current-mode biquad with three inputs and one output employing ‘‘only one’’ active element, a fully differential second-generation current conveyor (FDCCII), that is ‘‘two fewer’’ current conveyors than the recent proposed by [4-7]. Besides the proposed configuration employing only grounded capacitors and has no need of component matching conditions to realize all standard biquad filters this is unlike biquad

reported in [8].

Ⅱ. Circuit Description

The proposed novel current-mode universal biquad filter with three inputs and one output employing a single FDCCII is shown in Fig. 1. The proposed circuit comprises the minimum components: "only one" FDCCII, two grounded capacitors, and two resistors for realizing universal current-mode biquad. The use of only grounded capacitors makes the proposed circuit ideal for integrated circuit implementation [9, 10]. By using standard notation, the port relations of an FDCCII, which is a five-terminal analog building block, can be characterized by [11-13]

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Y4} \\ V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \\ I_{X+} \\ I_{X-} \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \tag{1}$$

Derive each nodal equation of the proposed circuit that the input-output relationship matrix form of Fig. 1 can be expressed as

$$\begin{bmatrix} sC_1 + G_1 & G_2 & 0 \\ -G_1 & sC_2 & 0 \\ -G_1 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ I_o \end{bmatrix} = \begin{bmatrix} I_{i2} + I_{i3} \\ I_{i1} \\ -I_{i3} \end{bmatrix} \tag{2}$$

From the above matrix form yields the following current transfer functions:

$$I_o = \frac{-I_{i3}(s^2C_1C_2 + G_1G_2) + I_{i2}(sC_2C_1) - I_{i1}(G_1G_2)}{s^2C_1C_2 + sC_2C_1 + G_1G_2} \tag{3}$$

Form equation (3), it is obvious that the proposed current-mode universal filter realizes the hig-pass, band-pass, low-pass, notch and all-pass filter responses indicated as follows:

(i) high-pass: $I_{i2}= 0$, and $I_{i1}= -I_{i3}=I_{in}$
(ii) band-pass: $I_{i3}= I_{i1}= 0$, and $I_{i2} = I_{in}$
(iii) low-pass: $I_{i2} =I_{i3} = 0$, and $I_{i1} = I_{in}$
(iv) notch: $I_{i1}= I_{i2}= 0$, and $I_{i3} =I_{in}$
(v) all-pass: $I_{i1}= 0$ and $I_{i2} = I_{i3} =I_{in}$

Note that no matching condition is required for the realization of the filter response.The natural angular frequency ω_o and the quality factor Q of the filter can be expressed as

$$\omega_o = \sqrt{\frac{G_1G_2}{C_1C_2}} \qquad Q = \sqrt{\frac{C_1G_2}{C_2G_1}} \tag{4}$$

The ω_o and Q sensitivities are given by

$$S_{G_1}^{\omega_0} = S_{G_2}^{\omega_0} = -S_{C_1}^{\omega_0} = -S_{C_2}^{\omega_0} = \frac{1}{2}, \text{ and } \; S_{C_1}^{Q} = -S_{C_2}^{Q} = S_{G_2}^{Q} = -S_{G_1}^{Q} = \frac{1}{2}$$

All passive sensitivities are small.

Taking into account the non-idealities of a FDCCII, namely,

$$\begin{bmatrix} V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & \beta_{11} & -\beta_{12} & \beta_{13} & 0 \\ 0 & 0 & -\beta_{21} & \beta_{22} & 0 & \beta_{24} \\ \alpha_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & \alpha_2 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \end{bmatrix} \tag{5}$$

where $\alpha_i = 1-e_i$ and e_i ($|e_i|<<1$) denotes the current tracking error and $\beta_v = 1-e_v$ and e_v ($|e_v|<<1$) denotes the differential voltage tracking error, respectively. The denominator of the transfer function is rewritten as

$$D(s) = s^2 C_1 C_2 + (1-\beta_{22}) s C_1 G_1 + \alpha_1 \alpha_2 \beta_{24} s C_2 G_1 + \alpha_2 \beta_{12} \beta_{24} G_1 G_2$$

The resonance angular frequency ω_o and the quality factor Q are obtained, respectively, by

$$\omega_o = \sqrt{\frac{\alpha_2 \beta_{12} \beta_{24} G_1 G_2}{C_1 C_2}} \tag{6}$$

$$Q = \frac{\sqrt{\alpha_2 \beta_{12} \beta_{24} C_1 C_2 G_1 G_2}}{(1-\beta_{22}) C_1 G_1 + \alpha_1 \alpha_2 \beta_{24} C_2 G_1} \tag{7}$$

Ⅲ.Simulation results

Finally, To verify the theoretical prediction of the proposed circuit, an H-Spice simulation, using the TSMC 0.5μm process with the parameters of level 49 technology tabulated in table 1, and the Matlab for the theoretical calculate to compare the results. The simulation circuit shown in Fig. 1 was built with $R_1 = R_2 = 15.9k\Omega$, and C_1=C_2=10pF, leading to a center frequency of $f_0 = 1MH_Z$ and quality factor of Q=1. The proposed fully differential second-generation current conveyor was constructed by the CMOS implementation. Fig. 2 shows a CMOS realization of extended FDCCII, the circuit is constructed mainly from the FDCCII reported in [12] with the additional transistors marked M37-M40 to account for the additional terminal of the extended FDCCII: Z-. The W/L of the transistors M37 and M38 are 240/2.4, and the transistors M39 and M40 are 60/2.4. The remaining transistors of the extended FDCCII have the same aspect rations as those in [12]. Its supply voltages and bias current were V_{DD}=-V_{SS}=2.5V, V_{bp}=-V_{bn}=1V and I_B=I_{SB}=350μA, respectively. Fig. 3 shows the simulation response and the theoretical frequency behaviors of the amplitude- and phase-frequency characteristics of the proposed low-pass filter. Fig. 4 shows the simulation response and the theoretical frequency behaviors of the amplitude- and phase-frequency characteristics of the proposed band-pass filter. Fig. 5 shows the simulation response and the theoretical frequency behaviors of the amplitude- and phase-frequency characteristics of the proposed high-pass filter. Fig. 6 shows the simulation response and the theoretical frequency behaviors of the amplitude- and phase-frequency characteristics of the proposed notch filter. Fig. 7 shows the simulation response and the theoretical frequency behaviors of the amplitude- and phase-frequency characteristics of the proposed all-pass filter. As can be seen, they a close agreement between theory and simulation.

Ⅳ.Conclusions

By employing the FDCCII, we present a new universal current-mode filter with three inputs and one output. The proposed circuit employs two fewer current conveyors to realize the same universal current-mode filter in the literature [4-7]. The employment of grounded capacitors and has no need of component matching conditions to realize all standard biquad filters, which is unlike biquad reported in [8]. Moreover, the new circuit still offers the following advantages: (i) the employment of minimum

active and passive components, (ii) the employment of two grounded capacitors suitable for IC implementation, (iii) without any component matching conditions to realize all the five generic filter responses, (iv) high output impedance good for cascadability, and (v) low passive sensitivity performance. H-Spice simulations with TSMC 0.5 μ m process and ± 2.5 V supply voltages confirm the theoretical predictions.

References

[1] G. W. Roberts, and A. S. Sedra, "All current-mode frequency selective circuits," Electron. Lett., vol. 25, no. 12, pp. 759-761, 1989.

[2] C. M. Chang, and P. C. Chen, "Universal active current filter with three inputs and one output using current conveyors," Int. J. Electronics, vol. 71, no. 5, pp. 817-819, 1991.

[3] C. M. Chang, "Universal active current filter with three inputs and one output using plus-type CCIIs," Electron. Lett., vol. 33, no. 14, pp. 1207-1208, 1997.

[4] E. O. Günes, A. Toker, and S. Özoğuz, "Insensitive current-mode universal filter with minimum components using dual-output current conveyors," Electron. Lett., vol. 35, no. 7, pp. 524-525, 1999.

[5] A. Toker, S. Özoğuz, and C. Acar, "Current-mode KHN-equivalent biquad using CDBAs," Electron. Lett., vol. 35, no. 7, pp.1682-1683, 1999.

[6] C. M. Chang, T. S. Liao, T. Y. Yu, E. S. Lin, C. H. Teng, and C. L. Hou, "Novel universal current-mode filters using unity-gain cells," Int. J. Electronics, vol. 88, no. 1, pp. 23-30, 2001.

[7] H. Y. Wang, and C. T. Lee, "Versatile Insensitive Current-Mode Universal Biquad Implementation Using Current Conveyors," IEEE Trans. Circuits Syst. Pt-II, vol. 48, no. 4, pp. 409-413, 2001.

[8] R. K. Sharma, and R. Senani, "Universal current mode biquad using a single CFOA," Int. J. Electronics, vol. 91, no. 3, pp. 175-183, 2004.

[9] M. Bhusan, and R. W. Newcomb, "Grounding of capacitors in integrated circuits," Electron. Lett., vol. 3, no. 4, pp. 148-149, 1967.

[10] K. Pal, and R Singh, "Inductor-less current conveyor all-pass filter using grounded capacitors," Electron. Lett., vol. 18, no. 2, pp. 47, 1982.

[11] C. M. Chang, B. M. Al-Hashimi, H. P. Chen, S. H. Tu, and J. A. Wan, "Current mode single resistance controlled oscillators using only grounded passive components," Electron. Lett., vol. 38, no. 19, pp. 1071-1072, 2002.

[12] A. A. El-Adawy, A. M., Soliman, and H. O. Elwan, "A novel fully differential current conveyor and applications for analog VLSI," IEEE Trans. Circuits Syst. II, vol. 47, no. 4, pp. 306-313, 2000.

[13] J. W. Horng, C. H. Hou, C. M. Chang, H. P. Chou, C. T. Lin, and Y. H. Wen, "Quadrature oscillators with grounded capacitors and resistors using FDCCIIs," ETRI Journal, vol. 28, no. 4, pp. 486-494, 2006.

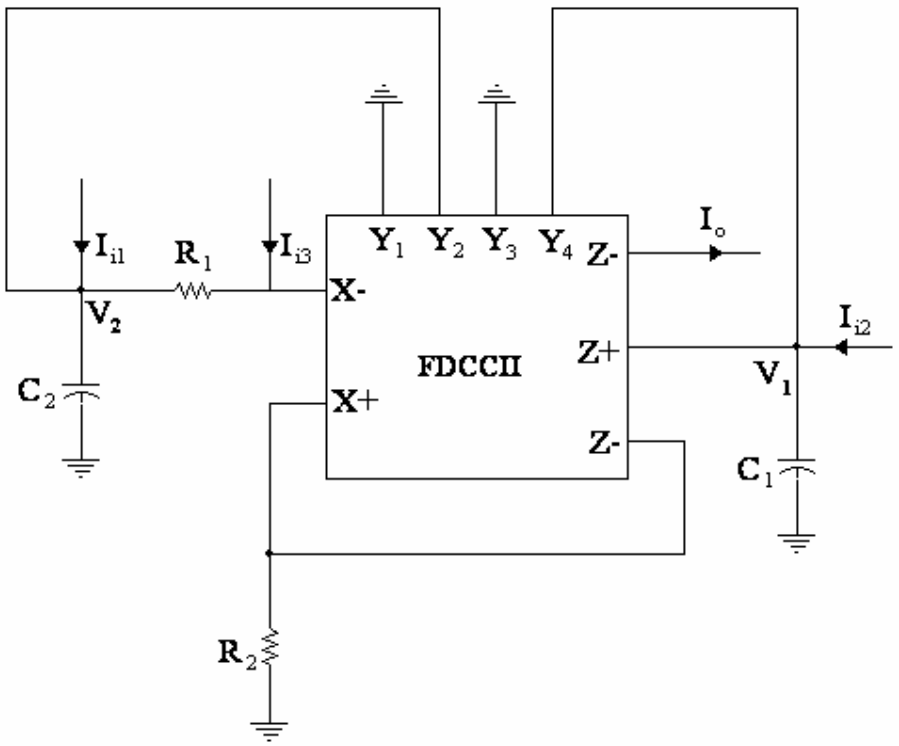

Fig. 1. Proposed universal current-mode biquad filter employing single FDCCII.

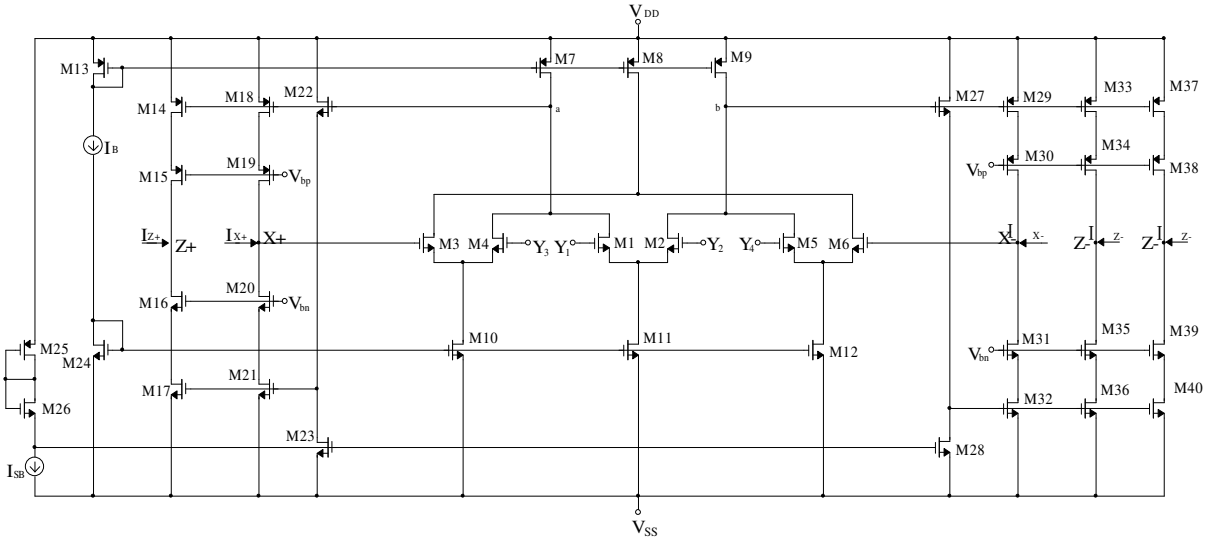

Fig. 2. The CMOS implementation of an extended FDCCII.

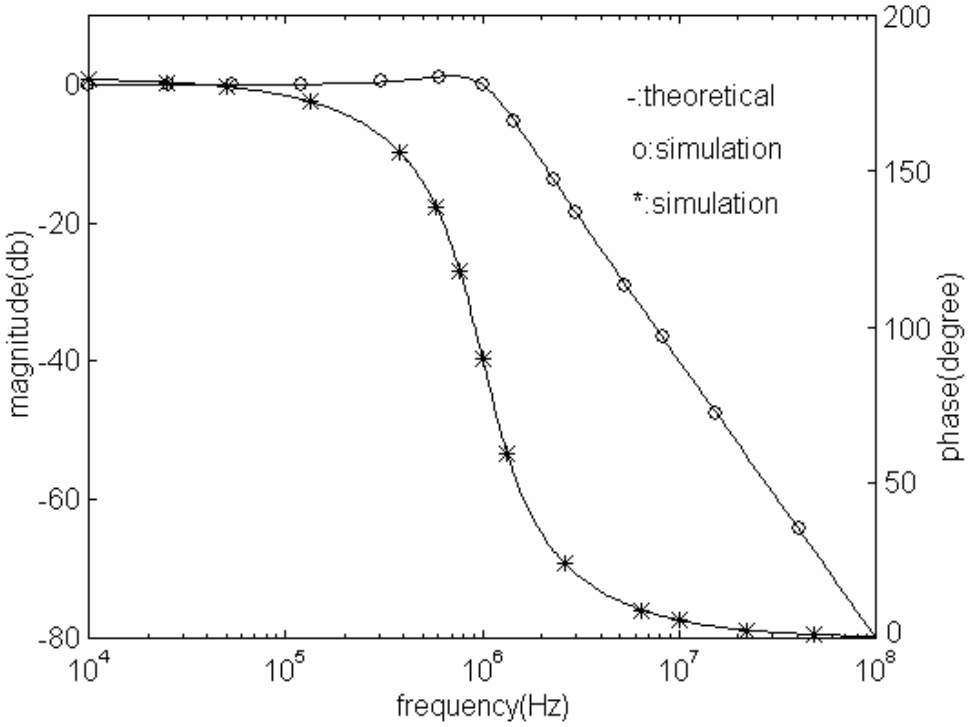

Fig. 3. Amplitude-frequency response and phase-frequency response of the proposed low-pass filter.

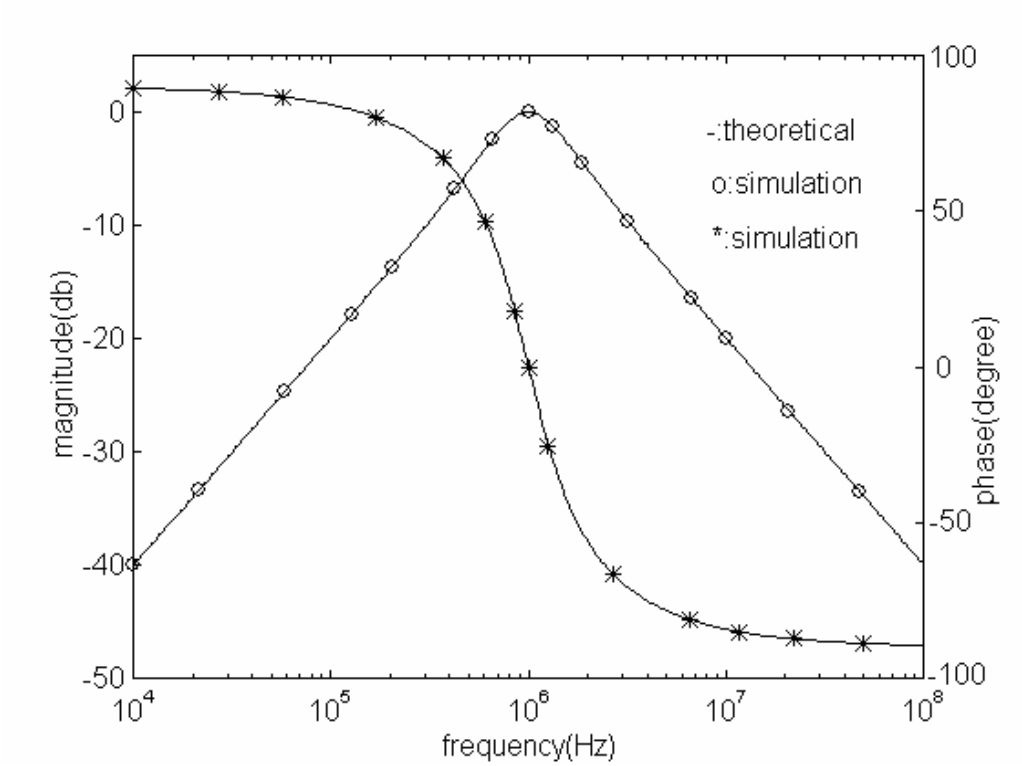

Fig. 4. Amplitude-frequency response and phase-frequency response of the proposed band-pass filter.

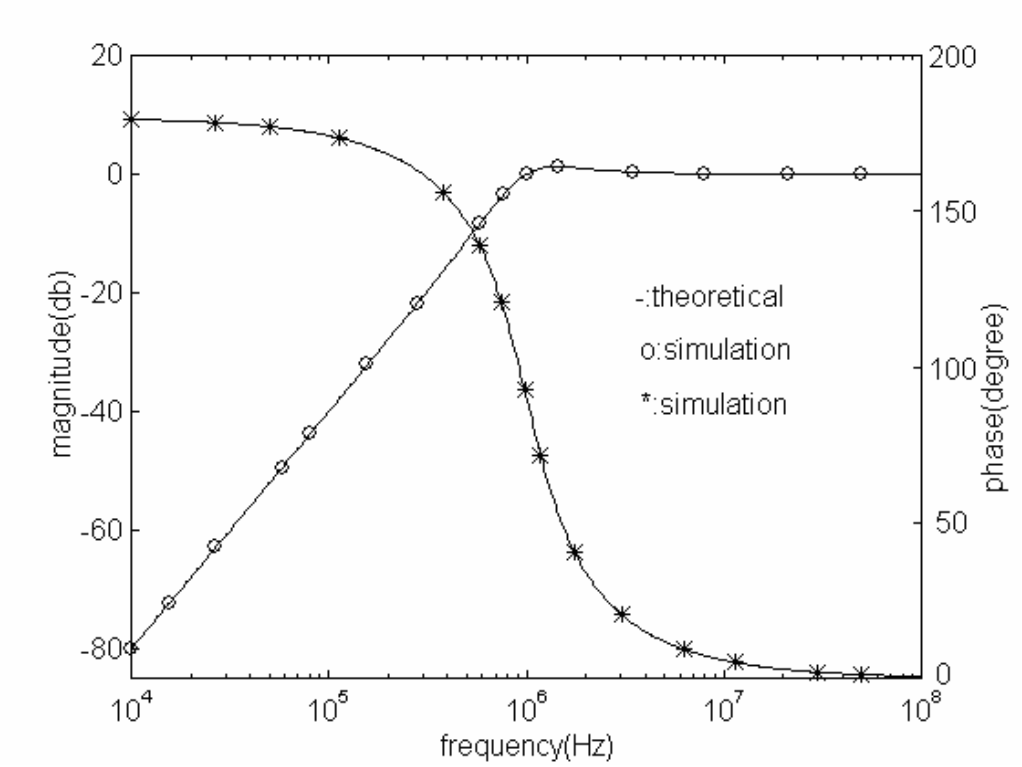

Fig. 5. Amplitude-frequency response and phase-frequency response of the proposed high-pass filter.

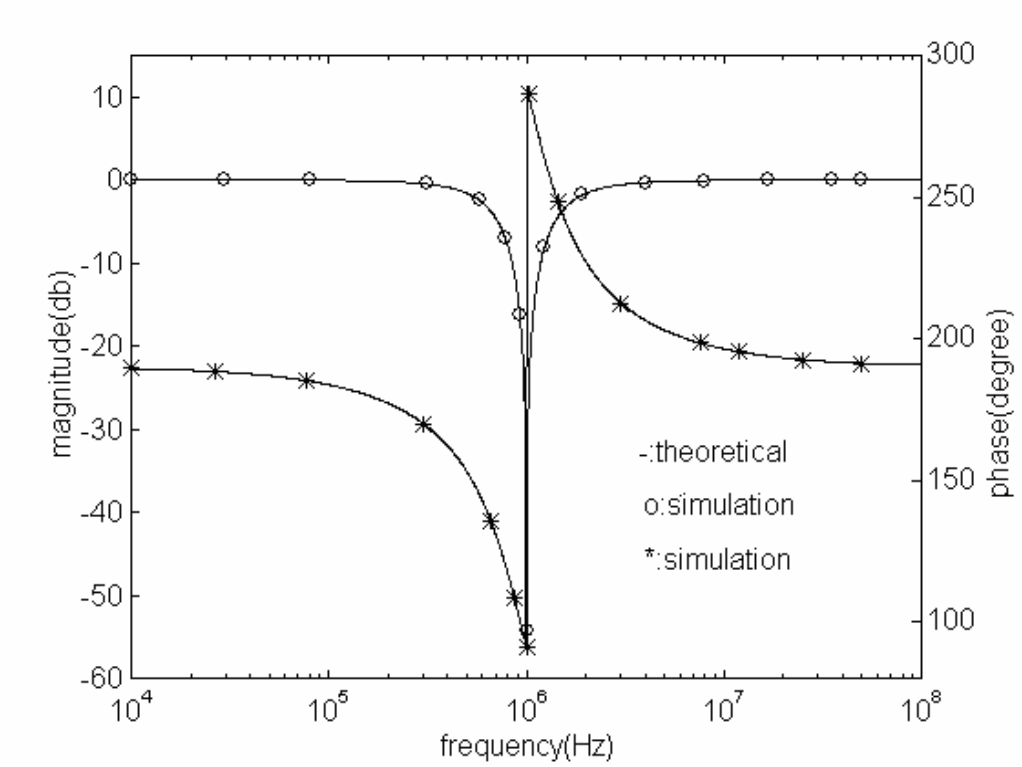

Fig. 6. Amplitude-frequency response and phase-frequency response of the proposed notch filter.

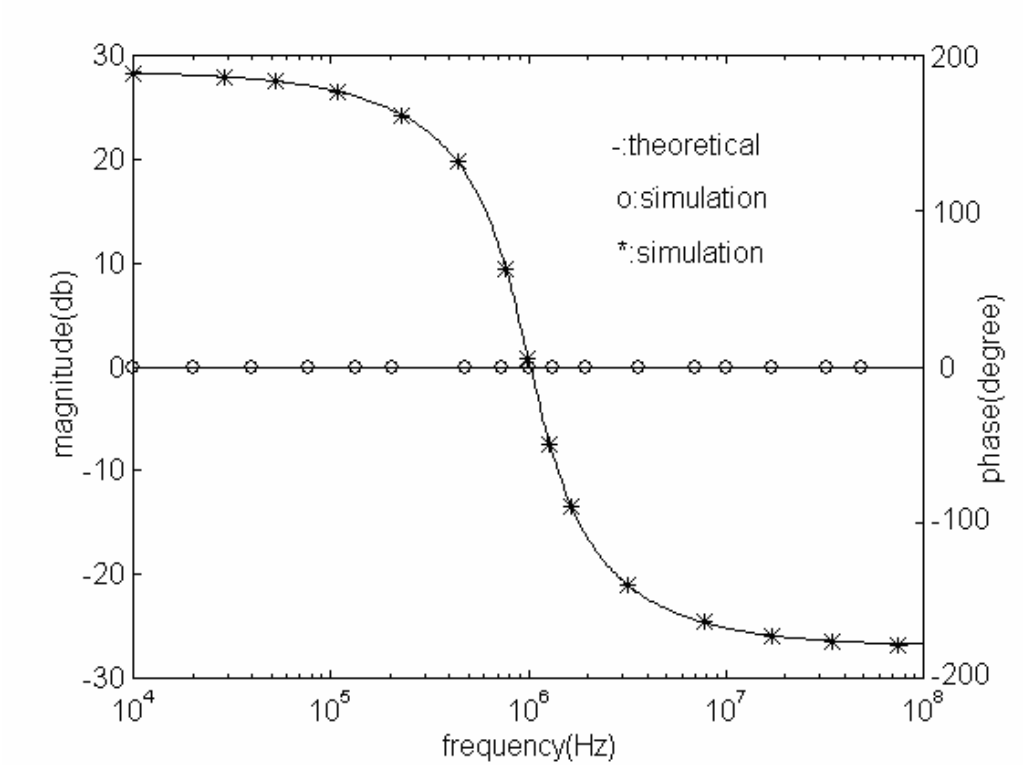

Fig. 7. Amplitude-frequency response and phase-frequency response of the proposed all-pass filter.

Table 1. Level 49 0.5 μ m TSMC CMOS parameters.

Model parameters of the NMOS device transistor		
+TNOM = 27	TOX = 1.35E-8	XJ = 2E-7
+NCH = 1.7E17	VTH0 = 0.8	K1 = 0.995618
+K2 = -0.0362332	K3 = 0.01	K3B = 2.84889
+W0 = 1E-6	NLX = 1E-8	DVT0W = 0.02
+DVT1W = 5.3E6	DVT2W = -0.0330119	DVT0 = 2.8
+DVT1 = 0.9	DVT2 = -0.05	U0 = 532
+UA = 9.34413E-10	UB = 6.94597E-19	UC = 7.56233E-11
+VSAT = 9.904058E4	A0 = 0.9793742	AGS = 0.145329
+B0 = 0	B1 = 1E-7	KETA = -0.0306332
+A1 = 0	A2 = 1	RDSW = 1.38431E3
+PRWG = 6.80401E-3	PRWB = 0.0616457	WR = 1
+WINT = 9.6E-8	LINT = 6.5E-8	DWG = -8.98745E-9
+DWB = 0	VOFF = -0.1193256	NFACTOR = 1.4537667
+CIT = 0	CDSC = 7.13148E-4	CDSCD= 0
+CDSCB = 0	ETA0 = 0	ETAB = 0
+DSUB = 0.0114564	PCLM = 1.5520328	PDIBLC1 = 0.7485143
+PDIBLC2 = 2.812824E-3	PDIBLCB = 0.0501264	DROUT = 0.9772589
+PSCBE1 = 5.087105E8	PSCBE2 = 5E-5	PVAG = 1.777713
+DELTA = 0.03	ALPHA0 = 0	BETA0 = 30
+RSH = 73.5273	JS = 1E-4	MOBMOD = 1
+PRT = 0	UTE = -1	KT1 = -0.3
+KT1L = 1.01856E-7	KT2 = 0.078502	UA1 = 4.2728E-9
+UB1 = -4.34101E-18	UC1 = -5.6E-11	AT = 3.3E4
+NQSMOD = 0	ELM = 5	WL = 2.06325E-23

+WLN = 0.599322	WW = 2.00911E-23	WWN = 1.45575
+WWL = -1E-20	LL = 2E-23	LLN = 0.981958
+LW = 2E-23	LWN = 1.11799	LWL = 4.36731E-21
+CAPMOD = 2	XPART = 0	CGDO = 1.4E-10
+CGSO = 1.4E-10	CJ = 8.97E-4	PB = 1.971
+MJ = 0.333	CJSW = 1.77E-10	PBSW = 0.275
+MJSW = 1.1	CGSL = 0	CGDL = 0
+CKAPPA = 0.6	CF = 0	CLC = 1E-7
+CLE = 0.6	WMIN = 5E-7	WMAX = 5E-5
+LMIN = 4E-7	LMAX = 5E-5	ACM = 2
+HDIF = 6E-7		
Model parameters of the PMOS device transistor		
+TNOM = 27	TOX = 1.35E-8	XJ = 2.5E-7
+NCH = 1.7E17	VTH0 = -0.978	K1= 0.4975752
+K2 = -1.508815E-4	K3 = 23.6093	K3B = -4.56804
+W0 = 1.987229E-7	NLX = 1E-8	DVT0W = 0.01
+DVT1W = 5.3E6	DVT2W = -0.032	DVT0 = 0.83
+DVT1 = 0.37	DVT2 = -0.558989	U0 = 242
+UA = 3.5398E-9	UB = 1E-21	UC = -7.08381E-11
+VSAT = 1.969491E5	A0 = 0.829709	AGS = 0.173707
+B0 = 3.49058E-7	B1 = 5.5064E-8	KETA = 5.35217E-4
+A1 = 0	A2 = 1	RDSW = 2.58577E3
+PRWG = 0	PRWB = 3.39081E-3	WR = 1
+WINT = 1.4E-7	LINT = -5.9E-8	DWG = 0
+DWB = 3.65377E-9	VOFF = -0.1192802	NFACTOR = 0.833819
CIT = 0	CDSC = 7.17652E-4	CDSCD = 0
+CDSCB = 4.0043E-4	ETA0 = 0.0305557	ETAB = 0
+DSUB = 0.12034	PCLM = 2.60508	PDIBLC1 = 9.759624E-4
+PDIBLC2 = 1.029842E-5	PDIBLCB = 0	DROUT = 1
+PSCBE1 = 8E8	PSCBE2 = 5E-5	PVAG = 0.961431
+DELTA = 0.01	ALPHA0 = 0	BETA0 = 30
+RSH = 190	JS = 1E-4	MOBMOD = 1
+PRT = 2.06325E-3	UTE = -1.001	KT1 = -0.264561
+KT1L = -1.03666E-7	KT2 = 0	UA1 = 2.7297E-9
+UB1 = -5.19208E-18	UC1 = -9.99137E-11	AT = 1.00316E3
+NQSMOD = 0	ELM = 5	WL = -1.26578E-14
+WLN = 1	WW = -5.45112E-14	WWN = 1
+WWL = 0	LL = 1.45297E-14	LLN = 1
+LW = 0	LWN = 1	LWL = 0
+CAPMOD = 2	XPART = 0	CGDO = 1.25E-10
+CGSO = 1.25E-10	CJ = 7.9E-4	PB = 0.885
+MJ = 0.552	CJSW = 2.75E-10	PBSW = 0.425
+MJSW = 0.2	CGSL = 0	CGDL = 0
+CKAPPA = 0.6	CF = 0	CLC = 1E-7
+CLE = 0.6	WMIN = 5E-7	WMAX = 5E-5
+LMIN = 4E-7	LMAX = 5E-5	ACM = 2
+HDIF = 6E-7		